

ABSTRACT

Methods, systems and program products are disclosed for selectively scaling an integrated circuit (IC) design: by layer, by unit, or by ground rule, or a combination of these. The selective scaling technique can be applied in a feedback loop with the manufacturing system with process and yield feedback, during the life of a design, to increase yield in early processes in such a way that hierarchy is preserved. The invention removes the need to involve designers in improving yield where new technologies such as maskless fabrication are implemented.